# AUTOMATIC CALIBRATION OF A MASKING PROCESS SIMULATOR

## FIELD OF THE INVENTION

The present invention relates to the field of semiconductor processing and more particularly to an improved process for automatically calibrating a masking process simulator.

## BACKGROUND OF THE INVENTION

An integrated circuit is fabricated by translating a circuit design or layout to a semiconductor substrate. In optical lithography, the layout is first transferred onto a physical template, which is in turn used to optically project the layout onto a silicon wafer. In transferring the layout to a physical template, a mask is generally created for each layer of the integrated circuit design. The patterned photomask includes transparent, attenuated phase shifted, phase shifted, and opaque areas for selectively exposing regions of the photoresist-coated wafer to an energy source. To fabricate a particular layer of the design, the corresponding mask is placed over the wafer and a stepper or scanner machine shines a light through the mask from the energy source. The end result is a semiconductor wafer coated with a photoresist layer having the desired pattern that defines the geometries, features, lines and shapes of that layer. The photolithography process is typically followed by an etch process during which the underlying substrate not covered or masked by the photoresist pattern is etched away, leaving the desired pattern in the substrate. This process is then

repeated for each layer of the design.

Ideally, the photoresist pattern produced by the photolithography process and the substrate pattern produced by the subsequent etch process would precisely duplicate the pattern on the photomask. For a variety of reasons, however, the photoresist pattern remaining after the resist develop step may vary from the pattern of the photomask significantly. Diffraction effects and variations in the photolithography process parameters typically result in critical dimension (CD) variation from line to line depending upon the line pitch of the surrounding environment (where pitch is defined for purposes of this disclosure as the displacement between an adjacent pair of interconnect lines). In addition to CD variation, fringing effects and other process variations can result in end-of-line effects (in which the terminal end of an interconnect line in the pattern is shortened or cut off by the photolithography process) and corner rounding (in which square angles in the photomask translate into rounded corners in the pattern). These three primary optical proximity effects, together with other photoresist phenomena such as notching, combine to undesirably produce a patterned photoresist layer that may vary significantly from the pattern of the photomask. In addition to variations introduced during the photolithography process, further variations and distortions are typically introduced during the subsequent etch process such that the pattern produced in the semiconductor substrate may vary from the photomask pattern even more than the photoresist pattern.

Conventional semiconductor process engineering in the areas of

photolithography and etch typically attempts to obtain a finished pattern that approximates the desired pattern as closely as possible by controllably altering the process parameters associated with the various masking steps. Among the parameters process engineers typically attempt to vary in an effort to produce a photoresist pattern substantially identical to the photomask pattern include the intensity, coherency and wave length of the energy source, the type of photoresist, the temperature at which the photoresist is heated prior to exposure (pre-bake), the dose (intensity x time) of the exposing energy, the numerical aperture of the lens used in the optical aligner, the use of antireflective coatings, the develop time, developer concentration, developer temperature, developer agitation method, post bake temperature, and a variety of other parameters associated with the photolithography process. Etch parameters subject to variation may include, for example, process pressure and temperature, concentration and composition of the etch species, and the application of a radio frequency energy field within the etch chamber.

Despite their best efforts, however, semiconductor process engineers are typically unable to manipulate the photolithography and etch processes such that the photoresist and substrate patterns produced by the processes are substantially identical to the photomask pattern.

To avoid the time and cost of producing actual test wafers for every desired permutation of process parameters, computerized simulation of masking processes is employed to facilitate the optimization of a particular masking sequence and the generation of an optical proximity correction (OPC) distorted

photomask. Masking process simulators receive various inputs corresponding to the parameters of the photoresist and etch processes to be simulated and attempt to simulate the pattern that will be produced by the specified masking process given a particular photomask. Accordingly, computerization has significantly enhanced the process engineer's ability to characterize and optimize masking processes.

Nevertheless, it is typically impossible to adequately account for the multitude of parameters associated with a masking process despite the effort devoted to masking process characterization, the introduction of optical proximity correction techniques, and the emergence of sophisticated process simulation software. In other words, simulation programs are ultimately unable to account for the various parametric dependencies in a manner sufficient to predict the exact pattern that will be produced by any particular masking process and mask.

Accordingly, what is needed is a method and system for improving the prediction accuracy of masking process simulator software. The present invention addresses such a need.

## SUMMARY OF THE INVENTION

The present invention provides a method and system for improving the prediction accuracy of masking process simulators through automatic calibration of the simulators. The method and system include performing a masking process using a calibration mask and process parameters to produce a calibration pattern on a wafer. A digital image is created of the calibration

pattern, and the edges of the pattern are detected from the digital image using pattern recognition. Data defining the calibration mask and the process parameters are then input to a process simulator to produce an alim image estimating the calibration pattern that would be produced by the masking process. The method and system further include overlaying the alim image and the detected edges of the digital image, and measuring a distance between contours of the pattern in the alim image and the detected edges. Thereafter, one or more mathematical algorithms are used to iteratively change the values of the processing parameters input to the simulator until a set of processing parameter values are found that produces a minimum distance between the contours of the pattern in the alim image and the detected edges.

According to the method and system disclosed herein, the calibration effectively calibrates the process simulator to compensate for process variations of the masking process. Once the calibration is performed and actual mask data and the modified process parameters are input to the process simulator, the process simulator will produce an image that varies minimally from the actual pattern produced by the masking process.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagram showing a portion of a desired semiconductor pattern and the patterned layer resulting from the masking process.

FIG. 2 is a flow chart illustrating a process for calibrating a process simulator to compensate for process variations of the masking process in

accordance with a preferred embodiment of the present invention.

FIG. 3 is a block diagram of a web-enabled process simulation system in a preferred embodiment of the present invention.

FIG. 4 is an illustration of an example calibration mask pattern.

FIG. 5 is an illustration of an example SEM image produced by the masking process using the mask design shown in FIG. 4.

FIG. 6 is a diagram showing an alim image superimposed with the detected SEM edges.

FIG. 7 is a diagram illustrating a user interface screen produced by the calibration program in a preferred embodiment of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

The present invention relates to simulating semiconductor fabrication processes and a method for improving process simulators through automatic calibration. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiments and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features described herein.

Referring now to FIG. 1 a portion of a desired semiconductor pattern and the patterned layer resulting from the masking process is shown. The

semiconductor pattern shown in dashed lines includes various pattern elements 102a, and 102b (collectively referred to as pattern elements 102). Using the pattern, a masking process is used to create the patterned layer 131, comprising the actual elements 132. The patterned layer 131 may comprise, in alternative embodiments, a photoresist pattern produced by a photolithography process or a substrate pattern produced by an etch process.

As will be appreciated to those skilled in the art of semiconductor processing and design, elements 102 of semiconductor pattern includes various interconnect sections and pattern elements designed to achieve a desired function when the integrated circuit contemplated by the semiconductor fabrication process is completed. Typical elements 102 of a semiconductor pattern are substantially comprised of straight lines and square corners. For a variety of reasons, reproducing the exact image of semiconductor pattern in a production process is extremely complicated due to the large number of parameters associated with typical masking processes and further due to the unavoidable diffraction effects which inevitably result in some variations between the photomask used to produce a pattern and the pattern itself.

It is seen in FIG. 1 that the actual pattern 131 produced by a masking process varies from the desired semiconductor pattern 102. This discrepancy is shown in FIG. 1 as the displacement between the dashed lines of pattern elements 102a and 102b and the actual pattern elements 132a and 132b. Typically, the variations from the idealized pattern 102 include rounding of the corners and a shrinking of the line widths. It will be appreciated to those skilled

in the art of semiconductor processing that variations from the desired semiconductor pattern can contribute to lower processing yields, reduced reliability, reduced tolerance to subsequent misalignment, and other undesired effects.

As is well-known in the art, commercial masking process simulation software is available that is capable of producing a simulated estimate of the pattern that would be produced by a specified masking process using a given photomask. Examples of process simulation software include TSUPREM-4™ and Taurus-LRC™ by Synopsys, Inc. of Mountain View, California. Masking process simulators are useful for generating a large quantity of information concerning the effects of modifying various parameters associated with the process. Simulation is necessary to avoid the time and expense associated with producing actual test wafers for each proposed parameter modification.

Ultimately, the simulator will produce an estimate of the pattern, referred to as an aerial or latent image, that varies from the actual pattern produced by the masking process (due to diffraction effects and variations in the masking process) regardless of the number of parameters incorporated into the simulator.

The Assignee of the present application has developed a process that improves the process simulator's prediction of the final pattern produced by a masking process by using the actual results obtained generated by the masking process. For example, U.S. Patent Nos. 6,078,738 and 6,081,659, which are hereby incorporated by reference, discloses a process that introduces a feedback mechanism into the simulation process whereby the discrepancies

observed between the actual pattern and the aerial image are analyzed to produce a modified simulator that results in less discrepancy, or error between the aerial image produced during a successive iteration of the simulator and the actual image produced by the pattern.

Using the actual results obtained by the masking process to improve the prediction accuracy of the process simulator program can be referred to as a calibration process. However, how the calibration is implemented, including how the simulator is modified based on the calibration, can significantly affect the performance of the simulator.

One approach for modifying the simulator during the calibration is a manual process whereby an operator iteratively changes the process parameter values input to the simulator by hand until the simulator achieves a desired level of performance. It is difficult, however, for the operator to change more than a couple of the processing parameter at a time, making the process tedious, error prone, and time-consuming.

Another calibration approach uses critical dimension checking whereby a critical dimension of a particular feature of the actual pattern produced by the masking process is measured directly from a production wafer. The same critical distance is also measured across the feature in the aerial image produced by simulator. The processing parameters input to the simulator are then changed using an exhaustive search algorithm until the simulator produces an aerial image that has a critical distance equal to that of the actual pattern. One disadvantage of this method is that the critical dimension typically measures a

feature in one dimension only, typically horizontally or vertically across the middle of the feature. The process, therefore, is incapable of analyzing the pattern in areas where most stepper errors occur, such as the ends of lines and the spaces between features.

Accordingly, the present invention provides an improved process for analyzing the difference between the aerial image produced by a simulator and the actual pattern produced by the masking process in order to provide an improved method for calibrating the simulator. According to the present invention, calibration mask data and process parameters are input to a process simulator to produce an aerial image estimating the calibration pattern that would be produced by a masking process. The same calibration mask data and process parameters are used during the masking process to produce an actual calibration pattern on a wafer. A digital image of the actual pattern on the wafer is obtained, preferably using a scanning electron microscope (SEM). The edges of the pattern are automatically recognized from the SEM image using pattern recognition, and the recognized edges of the actual pattern are superimposed with the pattern in the aerial image. The distance between the contours of the pattern in the aerial image and the countours of the SEM edges is then measured, providing a distance value that is based on two dimensions, rather than one. One or more mathematical algorithms are then used to iteratively change the values of processing parameters input to the simulator until a set of processing parameter values are found that produces a minimum distance between the aerial image contours and SEM edges. This new set of parameters

effectively calibrate the process simulator to compensate for process variations of the masking process.

Once the calibration is performed and an operator inputs actual mask data and the modified process parameters into the process simulator, the process simulator will produce an aerial image that varies minimally from the actual pattern produced by the masking process. The calibrated process simulator may be used for a variety of tasks including predicting mask defects, as a model for OPC correction, for phase shifting mask correction, and so on.

FIG. 2 is a flow chart illustrating a process for calibrating a process simulator to compensate for process variations of the masking process in accordance with a preferred embodiment of the present invention. The process begins in step 50 by providing a process simulation program that operates in accordance with the present invention on a server, and making the program available over a network, such as the Internet.

FIG. 3 is a block diagram of a web-enabled process simulation system in a preferred embodiment of the present invention. The simulation system 140 includes a process simulator 142 and an automatic calibration program 143 for calibrating the process simulator 142. The process simulator 142 and the automatic calibration program 143 are executed on a server 144 as application programs and accessed over a network 146 by one or more operators using client computers 150. The automatic calibration program 143 may be included as part of, or separate from the process simulator 142.

The process simulator 142 and calibration program 143 are capable of

accessing one or more mask layout databases 152, each of which includes a set of mask designs that will be used to fabricate a particular semiconductor device. In particular, the calibration process 143 typically accesses a calibration mask design (not shown) when calibrating the process simulator 142. The process simulation system 140 also includes a data set 154 defining the input processing parameters, as described below. FIG. 4 is an illustration of an example calibration mask pattern from the mask layout database 152. In a preferred embodiment, mask data is stored in GDSII format.

Referring again to FIG. 2, a calibration pattern is fabricated on a wafer by a masking process in step 52 whereby a physical calibration mask and a stepper machine are used to generate the calibration pattern under the conditions specified by the data set 154. The data set 154 includes global processing parameters that are associated with the masking process. In a preferred embodiment, the global processing parameters include both resist parameters for simulating the photoresist, and optical parameters for simulating the optics and characteristics of stepper machine.

As is well known to those skilled in the field of photolithography engineering, examples of resist parameters include resist contrast (gamma), resist thickness, resist sensitivity, resist solids content, and resist viscosity. Examples of the optical parameters that may affect the resist image include the intensity of the stepper lamp, the duration of the exposure, the coherency of the optical energy, the aperture of lenses, and the wavelength of the lamp source. It will be further appreciated to those skilled in the art, that the develop process and

the etch process both include a number of parameters that may also be input to the process simulator 142, such as develop time, developer concentration, developer temperature, developer agitation method, and any post bake time and temperature. Etch parameters may include, for example, etch temperature, etch pressure, and etchant composition and concentration. The process parameters described above are meant to be illustrative rather than exhaustive and additional parameters may be incorporated into the simulator 142.

After the physical calibration pattern is fabricated by the masking process, a scanning electron microscope (SEM) is used to create a digital representation of the pattern, referred to herein as an SEM image in step 54. FIG. 5 is an illustration of an example SEM image produced by the masking process using the mask design shown in FIG. 4.

Referring again to FIG. 2, according to one aspect of the present invention, in step 56, the edges of the mask pattern in the SEM image are automatically detected using pattern recognition. The detected edges may be stored in an edge database in a standard format, such as GDSII (a standard file format for transferring/archiving to the graphic design data). In one preferred embodiment, an algorithm, referred to as a Snake Algorithm, is used to automatically detect the mask edges from the SEM image, as disclosed in U.S. Patent Application Serial No. _____ entitled "Mask Defect Analysis for Both Horizontal and Vertical Processing Effects" (2513P) filed on ____ by the present assignee and herein incorporated by reference. In an alternative embodiment, an "Adaptive SEM Edge Recognition Algorithm" may also be used to detect the

edges, as disclosed in U.S. Serial No. _____, entitled "Adaptive SEM Edge Recognition Algorithm."

In step 58, the SEM image is correlated to the GDS mask design data layout database 152 in order to determine how many pixels in the SEM image are equal to one unit of measure of the mask design, which is typically nanometers.

In step 60, an operator of a client computer 150 invokes the calibration program 143. In step 62, the operator selects the calibration mask design and the data set 154 representing global processing parameters of the masking process that were used to fabricate a calibration pattern.

In step 64, the calibration mask data and process parameters are input to the process simulator 142 to produce an image estimating the calibration pattern that would be produced by a masking process. As is well-known in the art, an aerial or latent image may be produced by the simulator, which are collectively referred to herein as an "alim" image (**a**erial/latent **im**age). The alim images generated by the process simulator 142 may be stored either on a server, or on the client computer 150.

In step 66, the alim image, the calibration mask design, and the detected SEM edges are overlaid. In step 68, the alignment between the alim image, the calibration mask, and the detected SEM edges are refined. In a preferred embodiment, the alim image and the pattern in the SEM image may include corresponding alignment marks to facilitate a subsequent alignment and comparison. The overlaid images may optionally be displayed to the operator.

FIG. 6 is a diagram showing an example alim image 164, shown with white lines, superimposed with the detected SEM edges, shown with dark lines.

Referring again to FIG. 2, in step 70, the distance between the alim image contours and the detected SEM edges are determined. In a preferred embodiment, this distance is determined using a root mean square (RMS) algorithm. The RMS algorithm measures the distance between each pair of corresponding edges in the alim image 164 and the SEM image 166 (or a subset of the edges) and applies a weighted average to the measured distances to produce a single distance value. In another preferred embodiment, the weighted average is equal to an Nth root of an average Nth power of distance between the SEM edges and the alim image for some N not necessarily equal to 2. Calculating distances between the contours in this manner effectively provides a distance value that is based on two-dimensional measurements.

In step 72, one or more mathematical algorithms are used to search for a set of processing parameter values for input to the simulator that will produce the minimum distance between the alim image contours and the SEM edges. The operator may also define a minimum distance threshold that will be used to terminate the search, and the minimum and maximum possible values for the processing parameters.

In a preferred embodiment, a subset of the processing parameters used by the masking process are input to the mathematical algorithm. According to the present invention, the following 11 processing parameters are used to determine the minimum distance: focus, diffusion, sigma in, sigma out, angle of the pole

location, numerical aperture, sigma of the pole, spherical, coma_x, coma_y, and intenstity contour.

In step 74, it is determined if the calculated distance between the alim image contours and the SEM edges meets the minimum distance threshold set by the operator. The minimum distance threshold is dependent upon the particular process technology being used. For a 130 nm process technology, for example, the minimum distance threshold may be set at 8-10 nm, which means that the process simulator must produce an alim image 164 that is within 10% of an SEM image 166. For critical applications, an error threshold of 5% or less may be necessary.

If the calculated distance does not meet the minimum distance threshold, then the algorithm calculates new values for the processing parameters in step 76. The new processing parameter values are calculated during the process of minimizing the distance between the alim image contours and the SEM edge contours given a function (f) of the 11 variables (x):

$$f(x_1,\ldots,x_{11})/R^{11}\text{-}R$$

In a preferred embodiment, two algorithms are employed to minimize this equation. First, a well-known stochastic algorithm is used to iteratively change the processing values until a global minimum for the function is found. This first set of calculated parameter values that produce the global minimum are then input to a second well-know algorithm, referred to as a simplex or Powell algorithm. This algorithm begins with the function defined by this set of parameter values and iteratively changes the values of the parameters until local

minimums within the function are found, producing a second set of parameter values.

In step 78, this second set of calculated parameter values are input to the process simulator 142 to generate a new alim image 164, and the process continues with steps 66-72. The alim image 164 is overlaid with the SEM edges and the distance between the two are calculated, etc. If the calculated distance between the alim image contours and the SEM edge contours does not meet the minimum distance threshold in step 74, then the process continues. If the calculated distance between the alim image contours and the SEM edge contours meets the minimum distance threshold in step 74, then in step 80 the current set of parameter values are the optimal set of parameters and are output by calibration program 143 for calibration of the process simulator 142.

FIG. 7 is a diagram illustrating a user interface screen produced by the calibration program in a preferred embodiment of the present invention. In a further aspect of the present invention, the calibration program user interface screen 170 displays individual graphs 172 for each processing parameter that plot the parameter values for each iteration along the x-axis, and the resulting RMS distance value along the y-axis. In addition to the individual parameter graphs 172, the user interface screen also displays a global graph 174 plotting the global RMS distance result of each iteration.

A method and system for calibrating a process simulator have been disclosed. The present invention has been described in accordance with the embodiments shown, and one of ordinary skill in the art will readily recognize that

there could be variations to the embodiments, and any variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

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